


P45ZV10

GP104 - 8GB GDDR5X, 256b, 256Mx32
Tall DVI-D + DP + DP + DP/HDMI + DP

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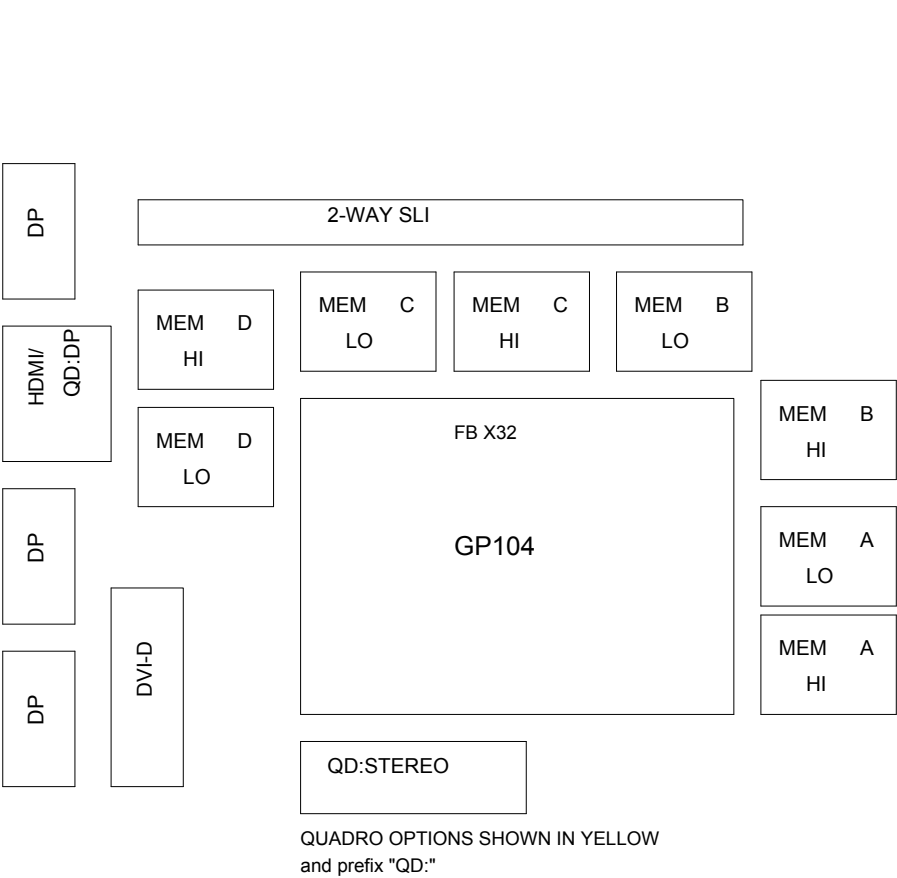
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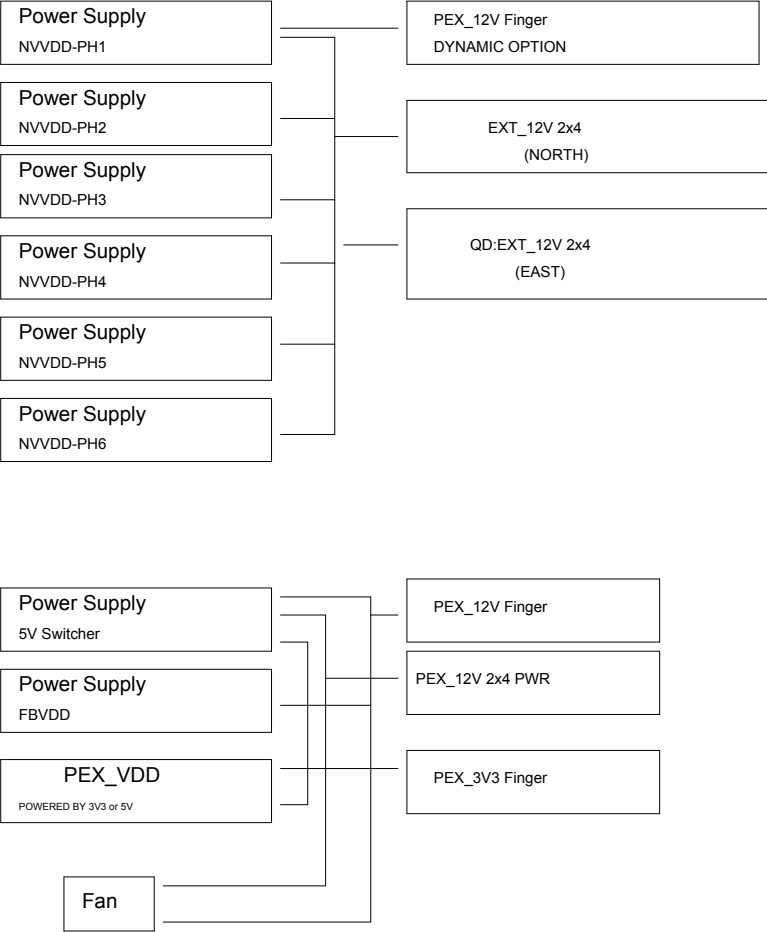


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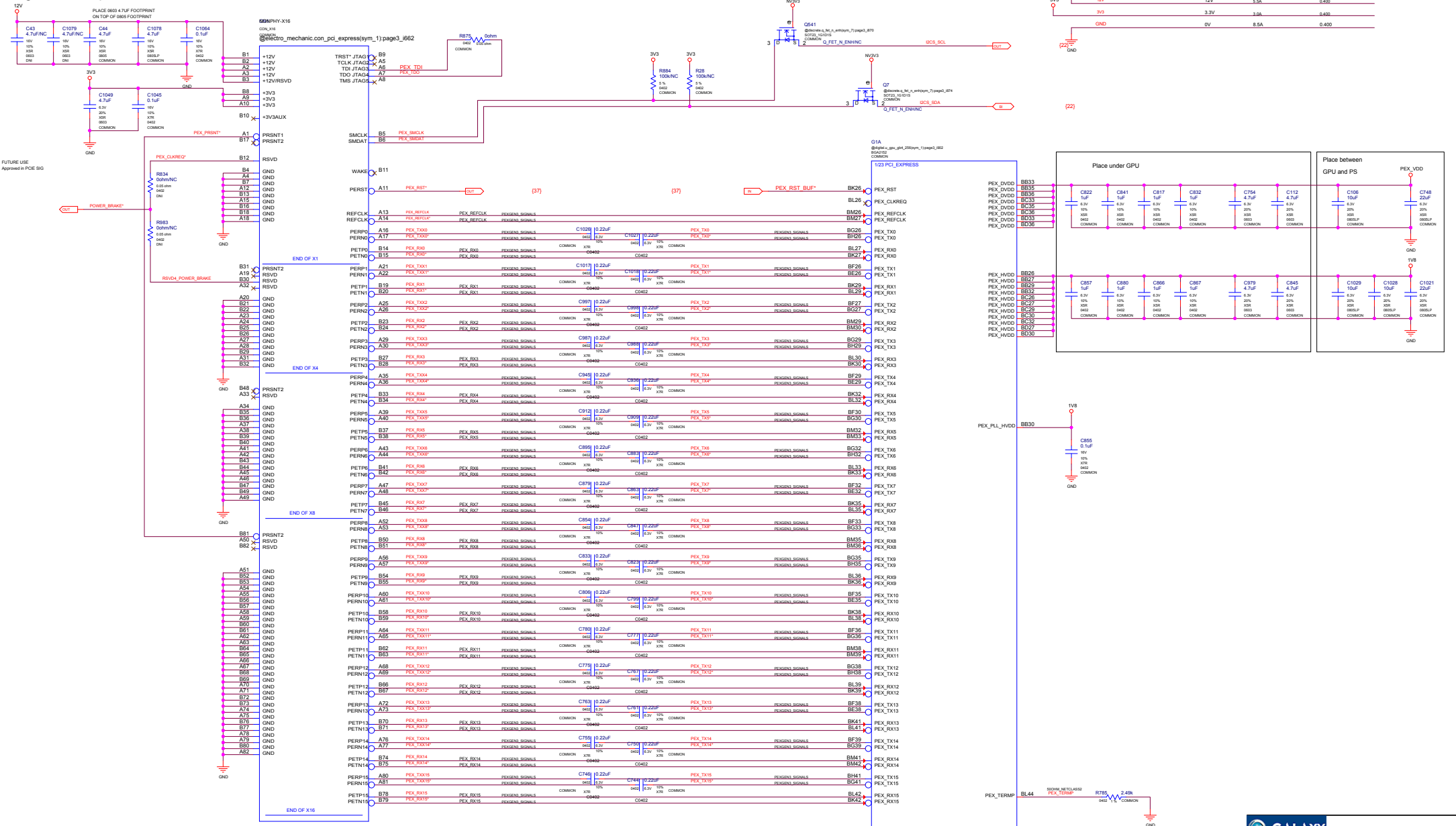
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and prefix "QD:"



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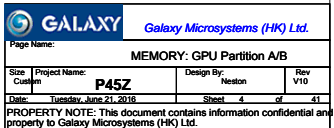
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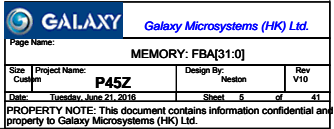


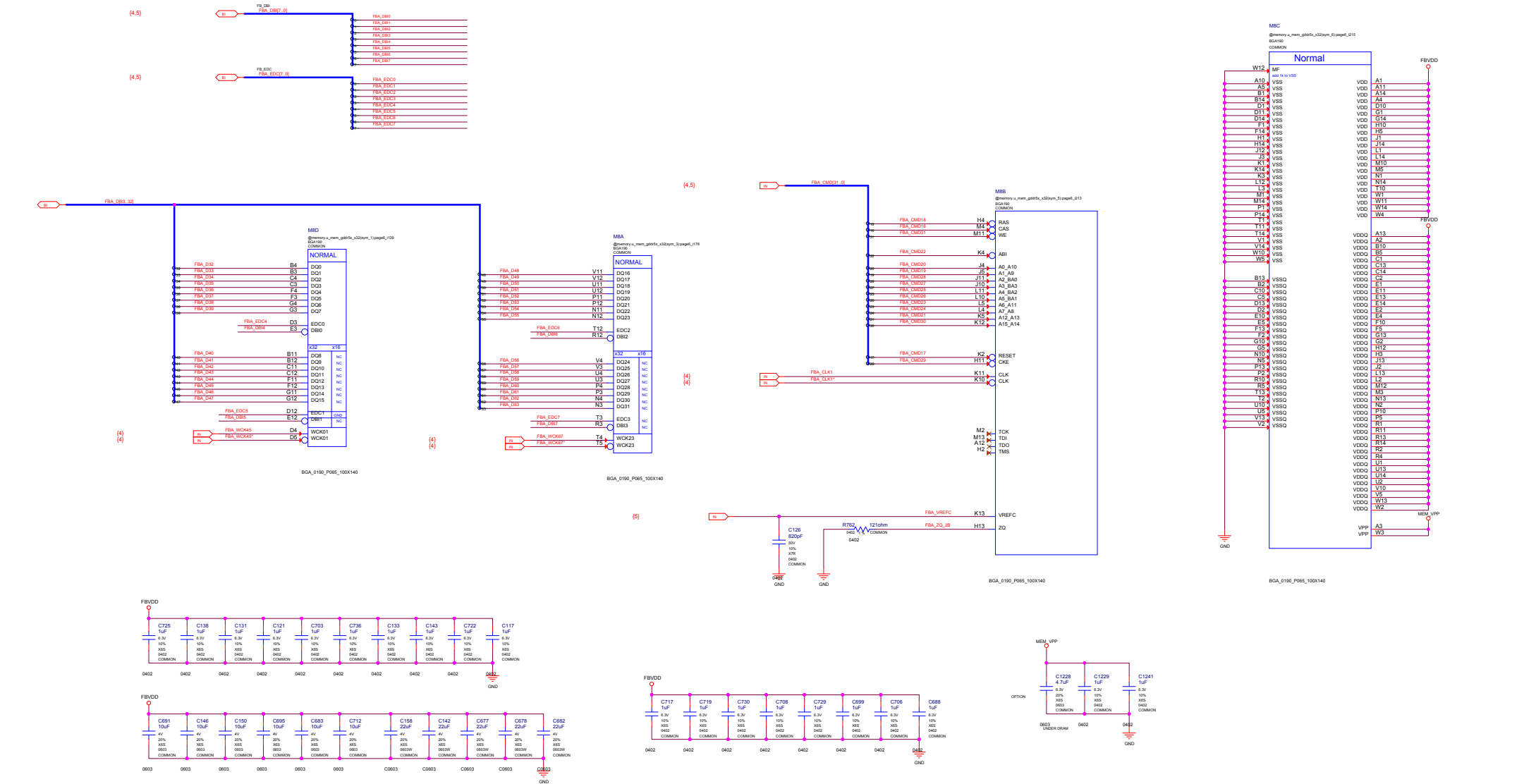
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

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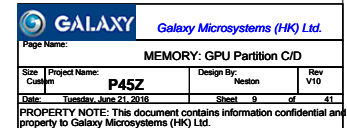
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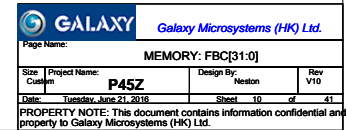
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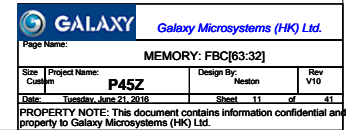
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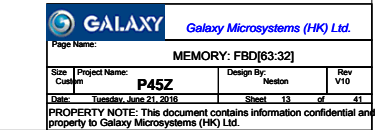
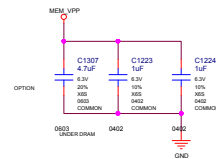
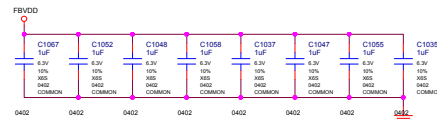
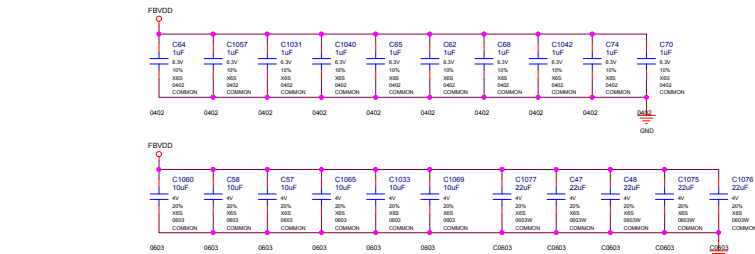
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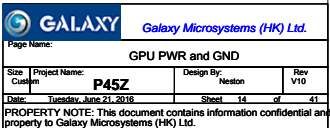




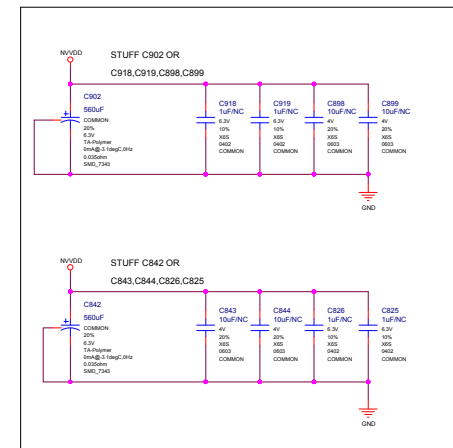
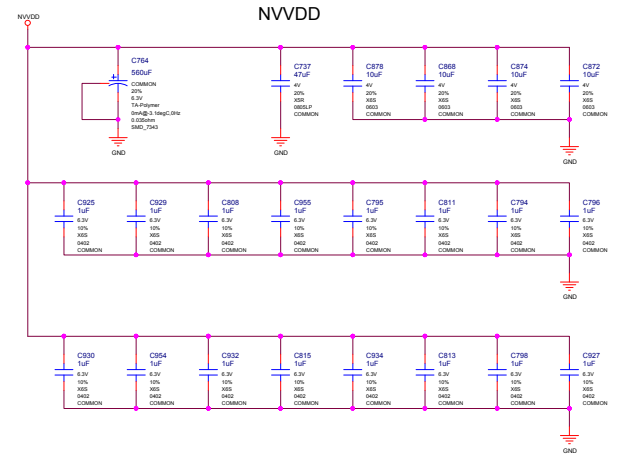
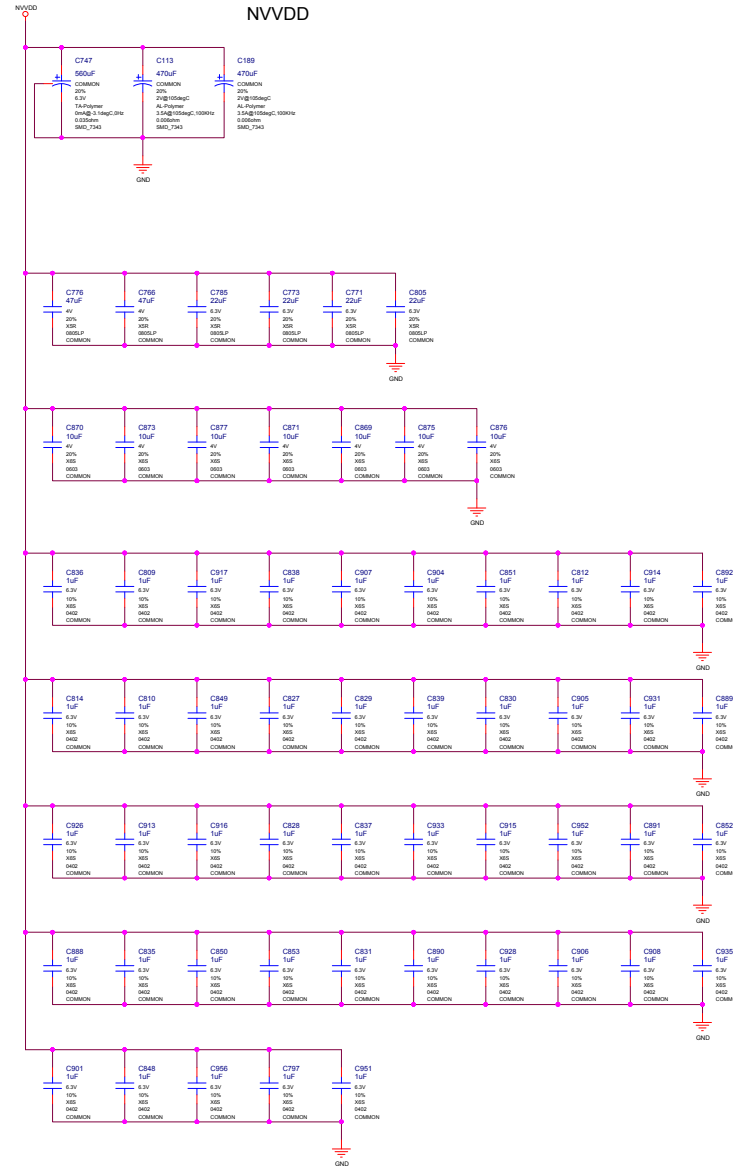
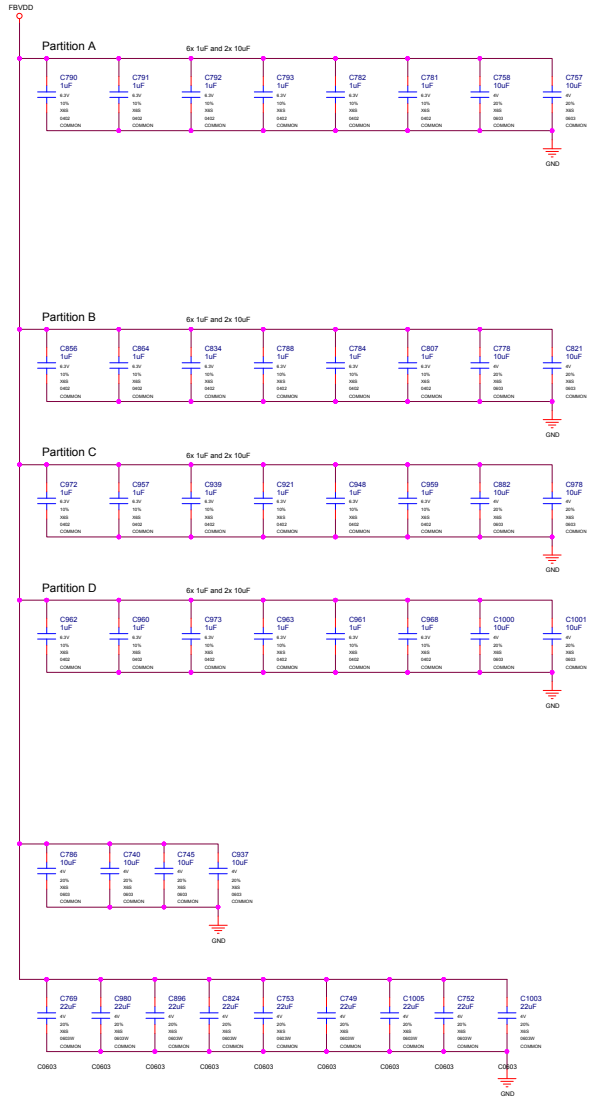




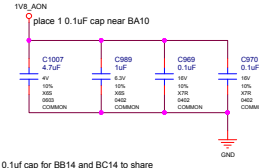




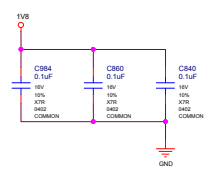
FBVDD

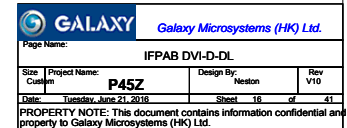


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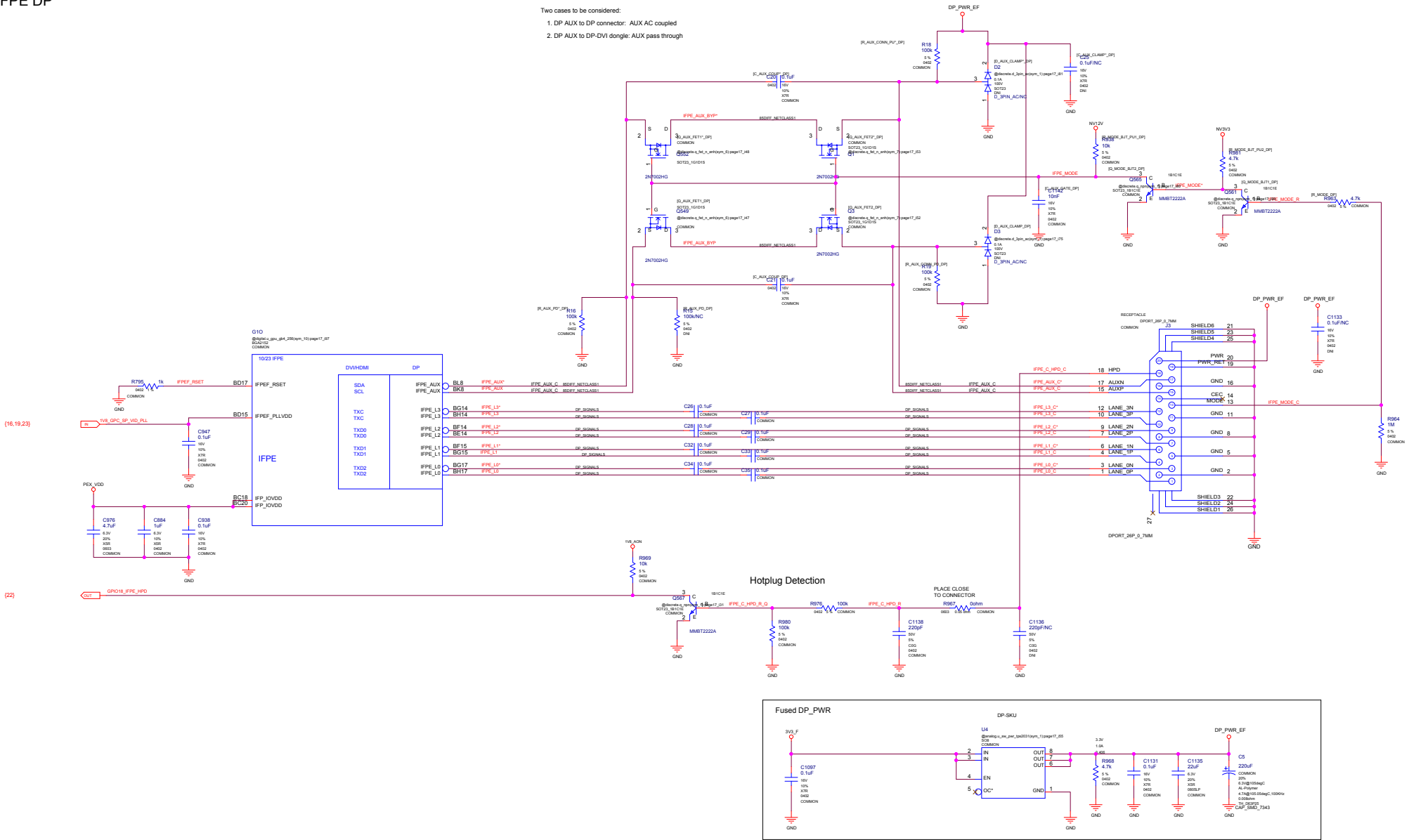


VDD18






- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

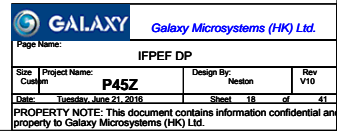


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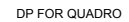
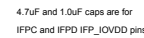
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PAGE DETAIL	IFPE DP


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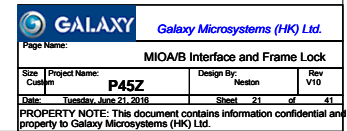
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

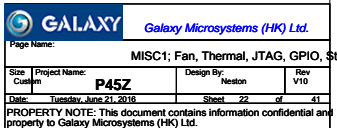


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IFPC HDMI 2.0/DP			
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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111

ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111	DEFAULT
L	L	L	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	0	1	0
L	H	M	1	0	1	1
L	M	H	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

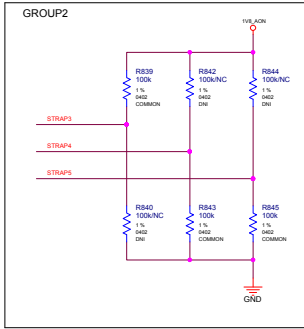
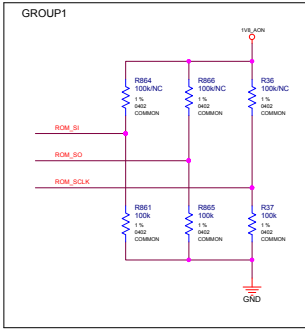
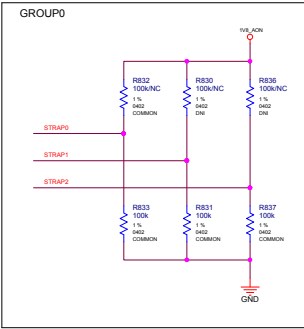
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

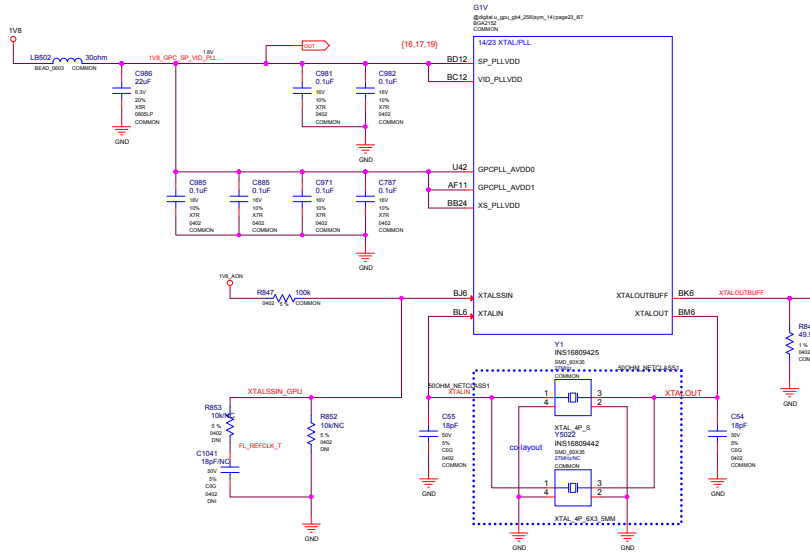
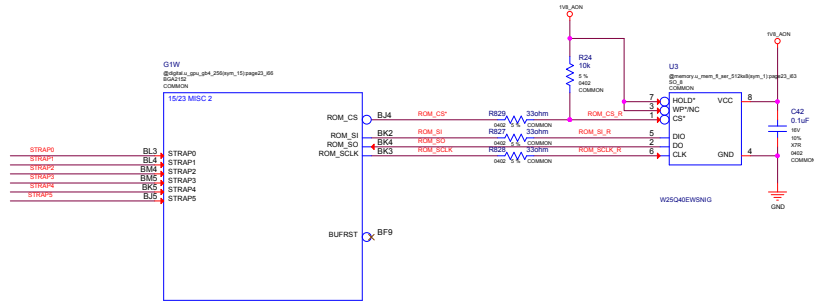
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



CFG[3:0]	Config	Width	Vendor
0000	256Mx32 256-bit Micron		
0001	Reserved		
0010	Reserved		
0011	Reserved		
0100	Reserved		
0101	Reserved		
0110	Reserved		
0111	Reserved		



XTALOUTBUFF		
1.8V	0.9V	0V
85% PWM	35% PWM	DISABLED (100%)

Page Name: MISC2: ROM, XTAL, Straps

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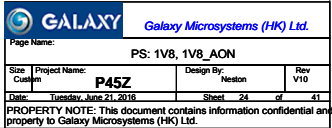
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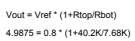
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5V 3/3 F



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A	B	C	D	E	F	G	H
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A	B	C	D	E	F	G	H
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VID Table

GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	1	0	0	1.1750V
0	0	1	0	1	1.1625V
0	0	1	1	0	1.1500V
0	0	1	1	1	1.1375V
0	1	0	0	0	1.1250V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V

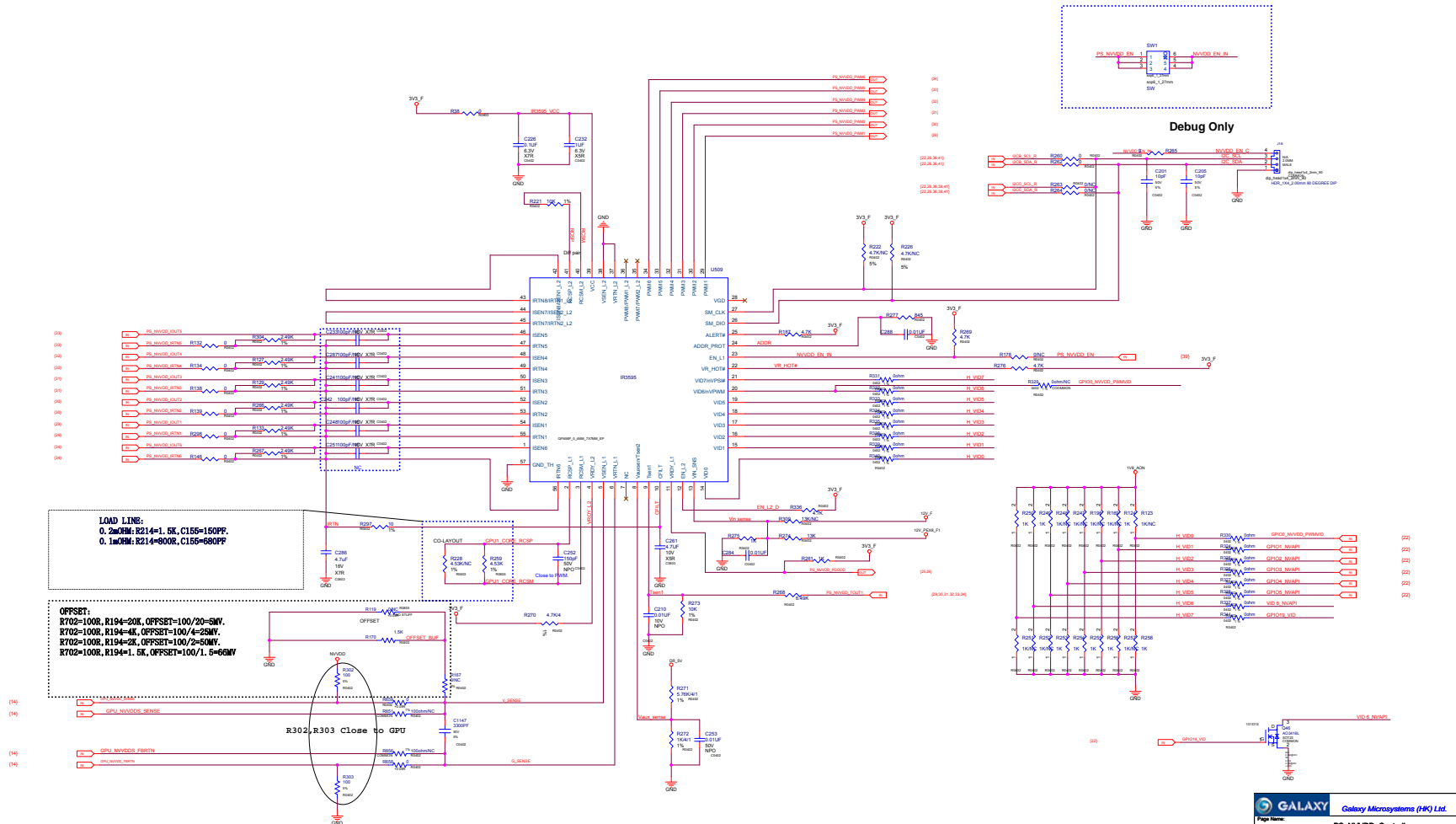
SOFT START (VR11)

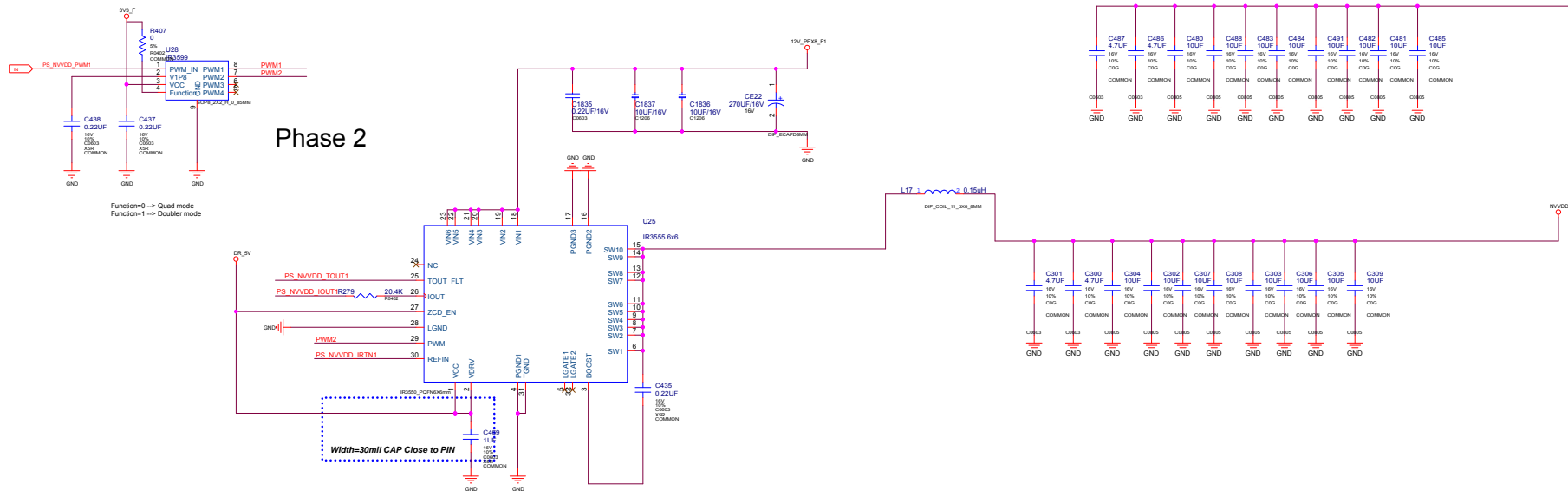
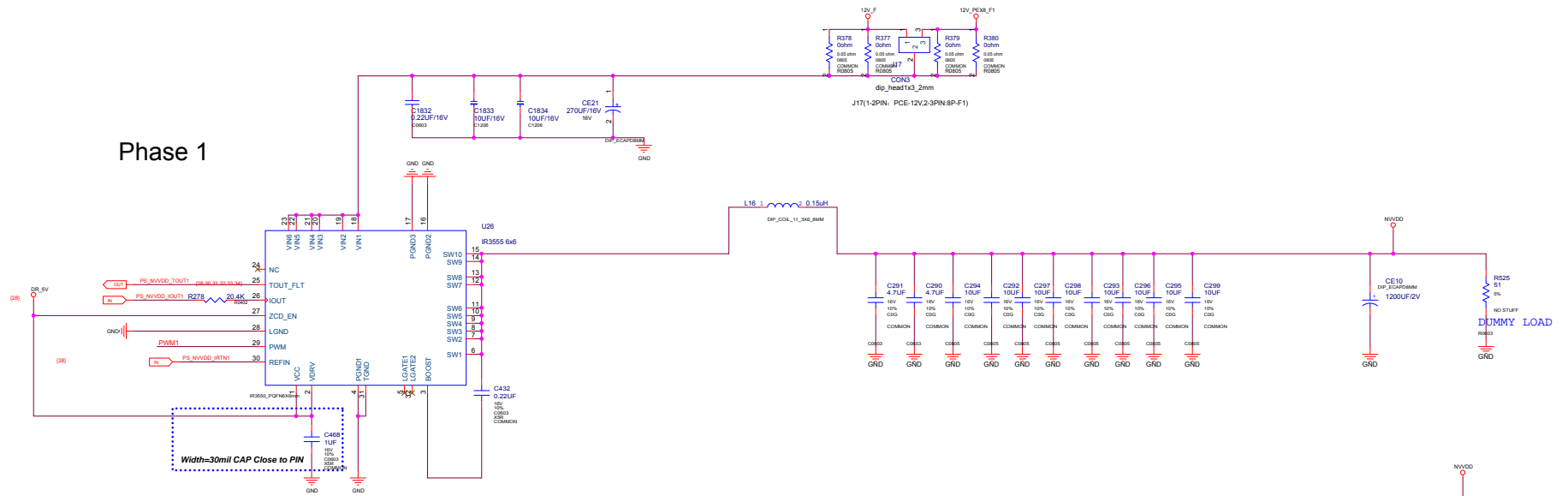
1. Ramp DV to 1.15V in ~2ms
2. Hold at 1.15V for ~150us
3. Read VID
4. VDD set to 0.9V during GPIO 10-state

VID[5:7] to 1001 to set 0.9V

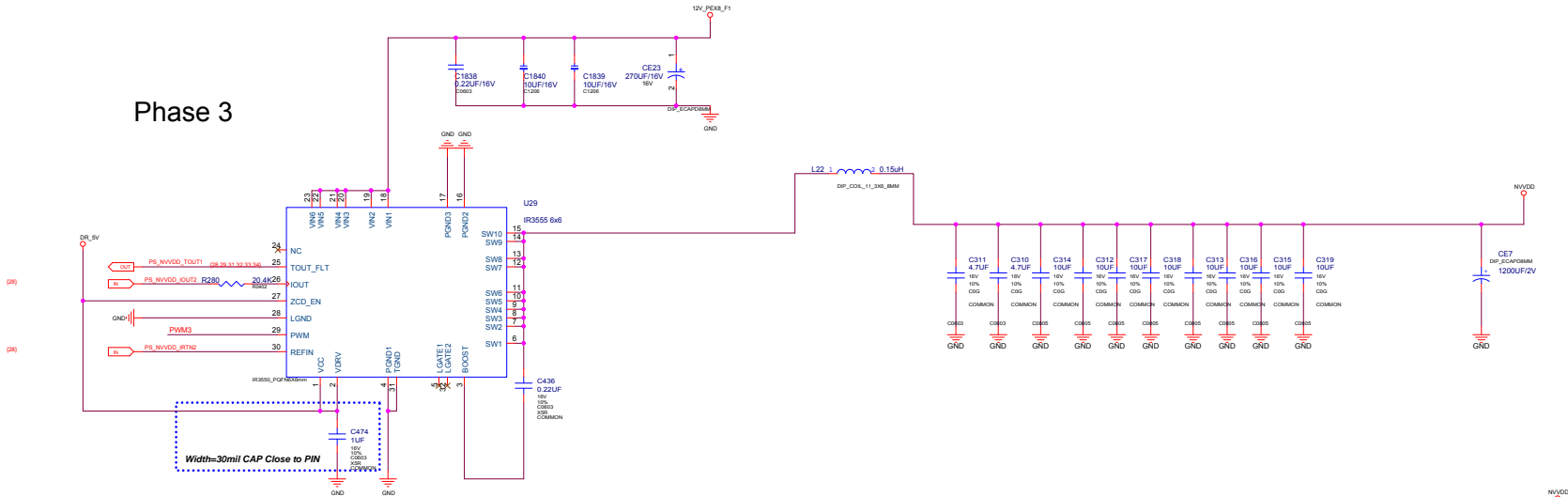
P-STATE VOLTAGES

1. PG at 1.05V to 1.15V (depending on VB)
2. PBP12 at 0.80V

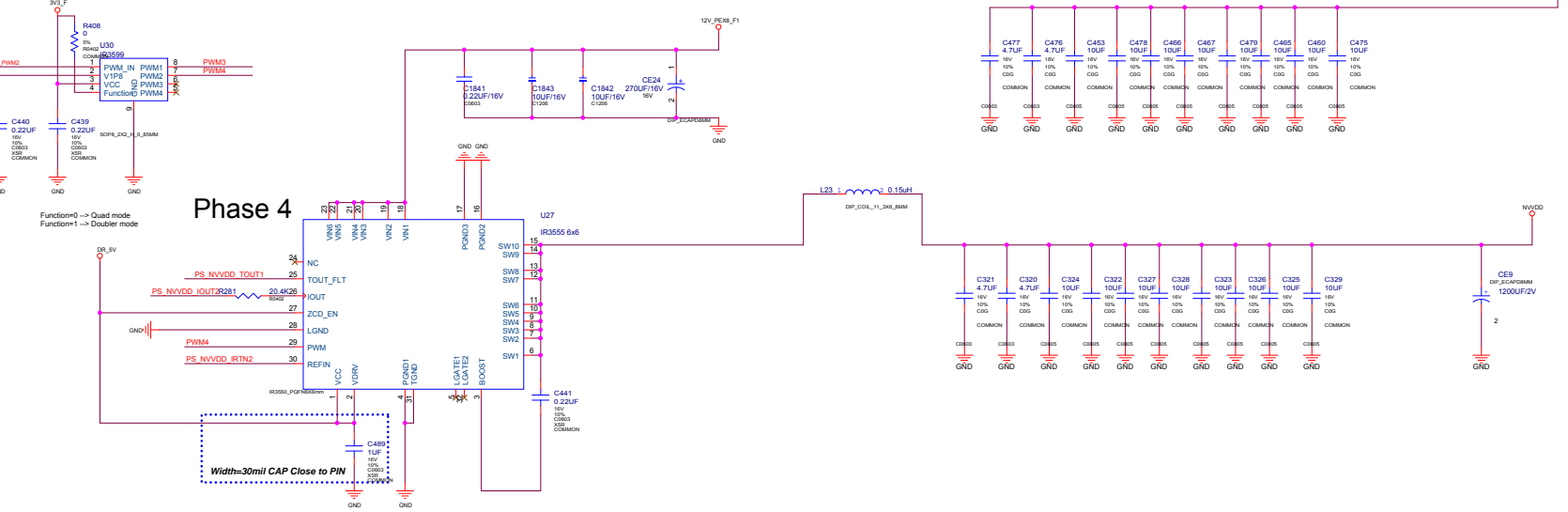




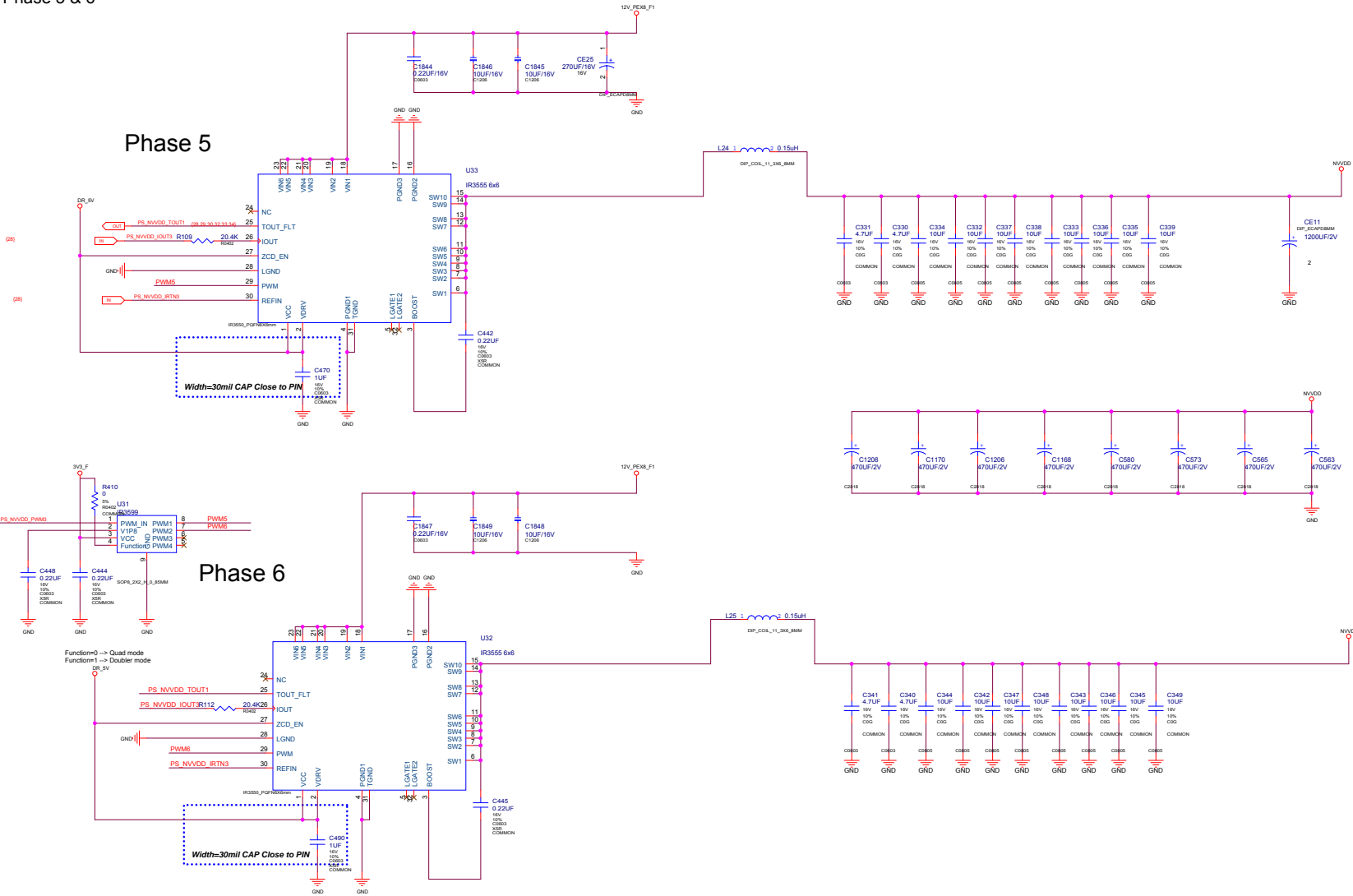
Phase 3



Phase 4




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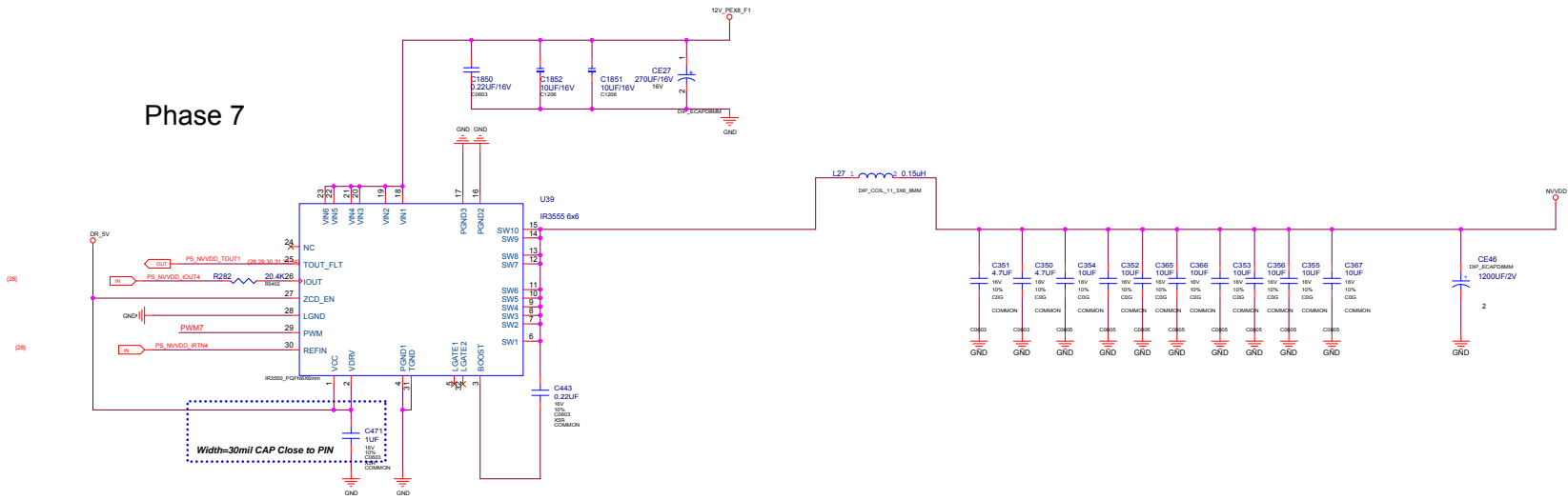


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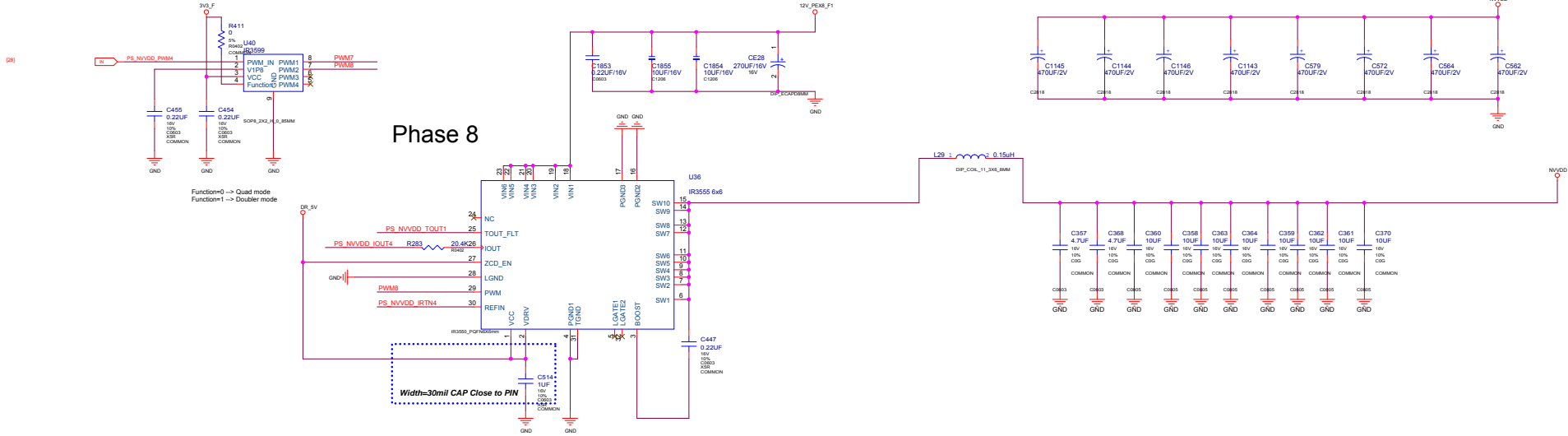
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PAGE DETAIL	PS: NVVDD Phase 5 & 6

			
Page Name: PS: NVVDD Phase 5 & 6			
Size: C452	Project Name: P45Z	Design By: Nelson	Rev: V10
Date: Tuesday, June 21, 2018	Sheet 31 of 41		
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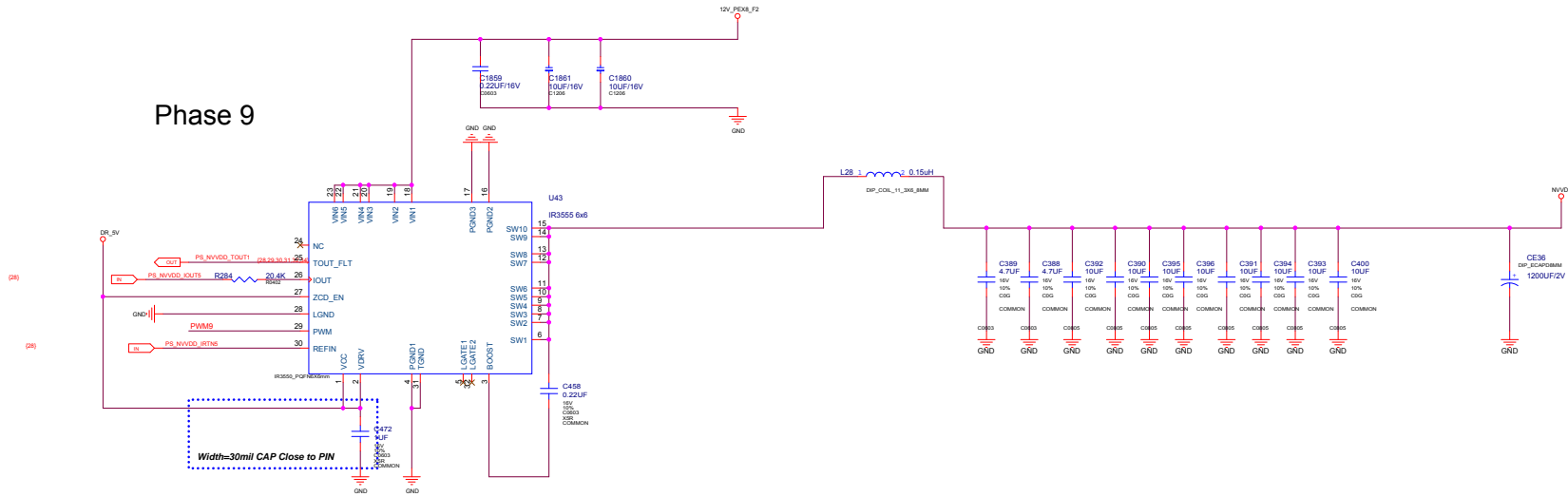
Phase 7



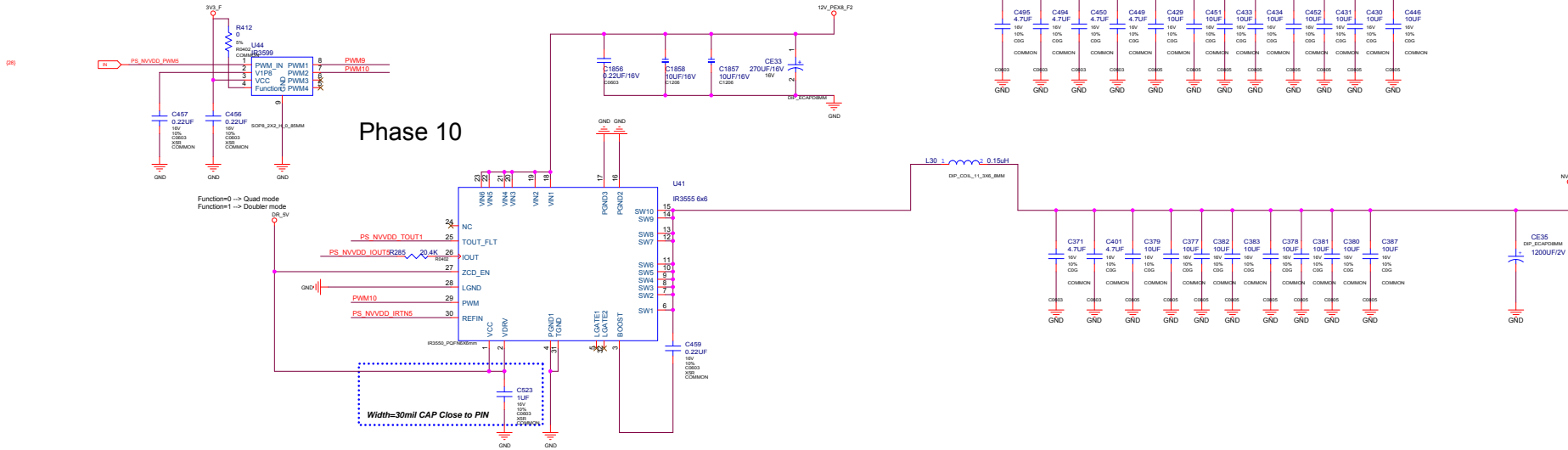
Phase 8



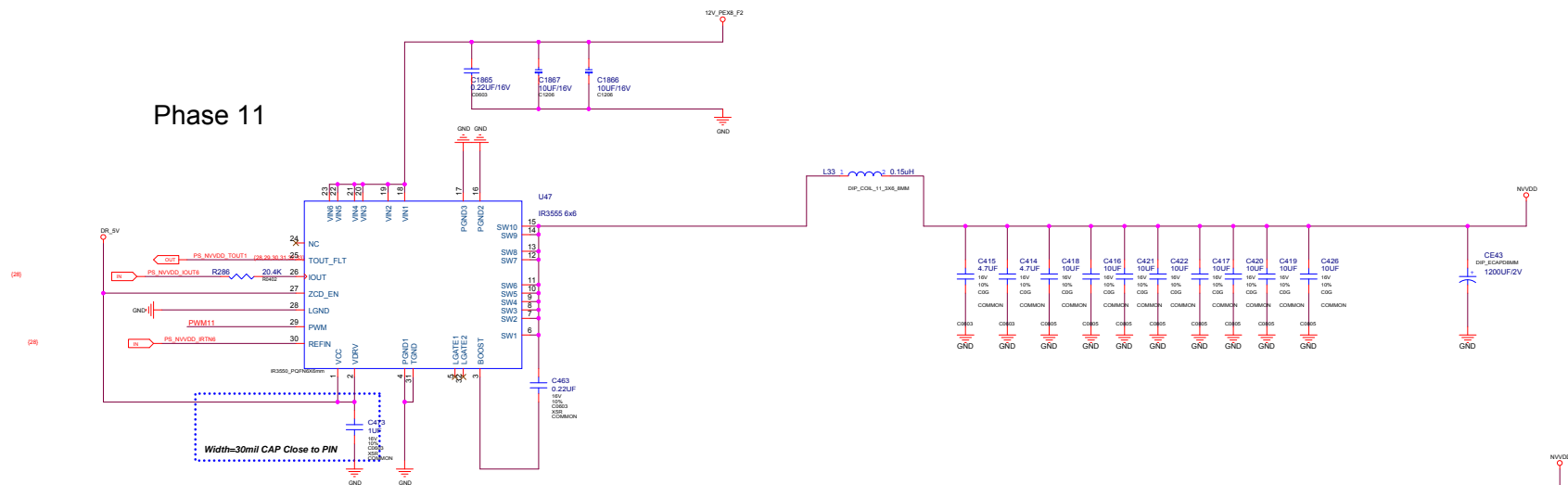
Phase 9



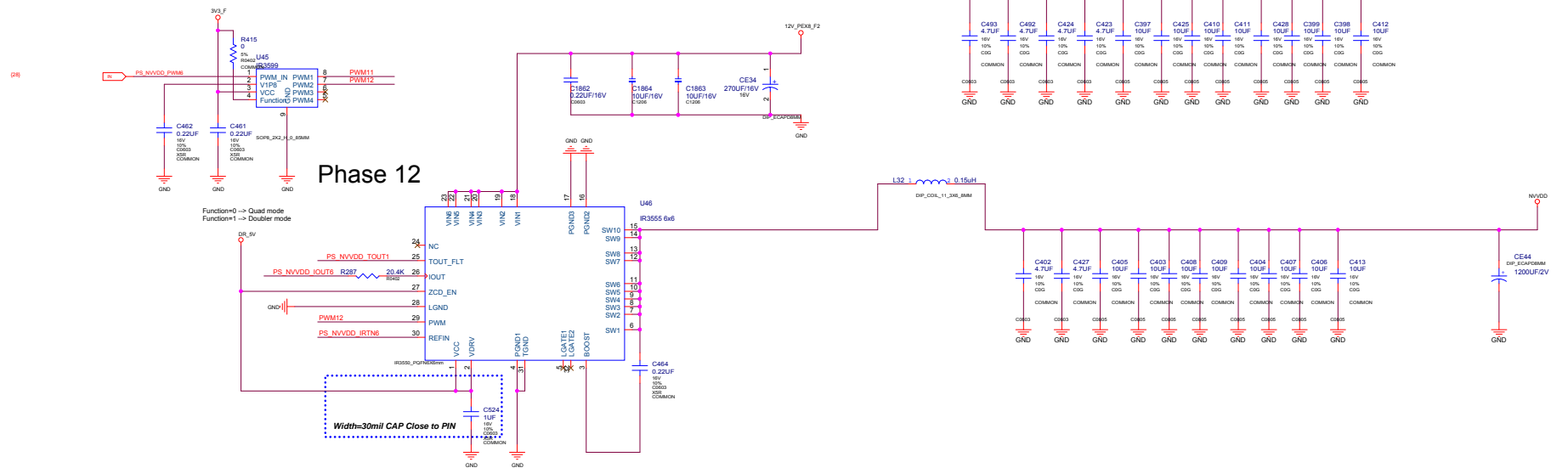
Phase 10

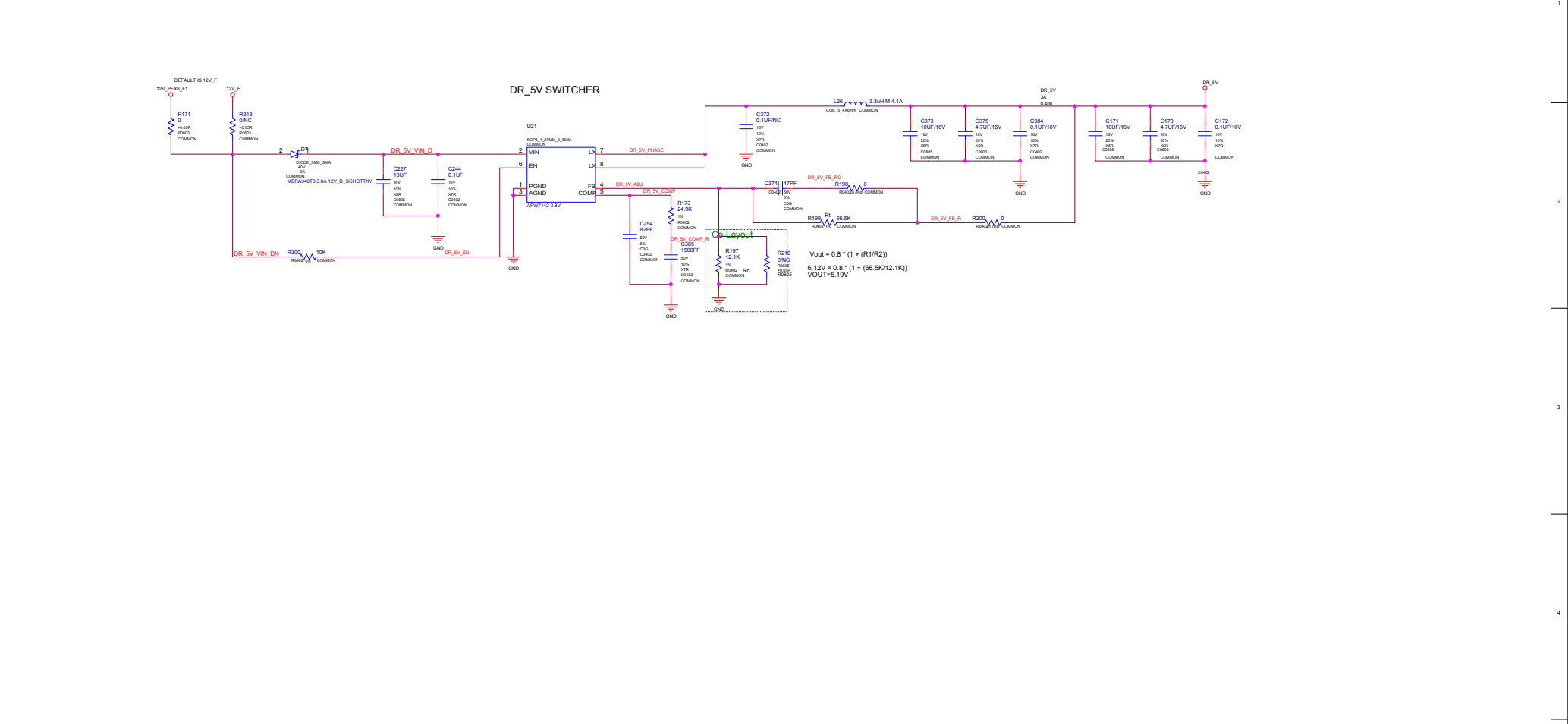


Phase 11



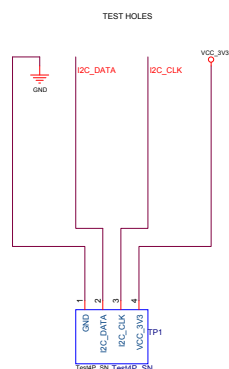
Phase 12



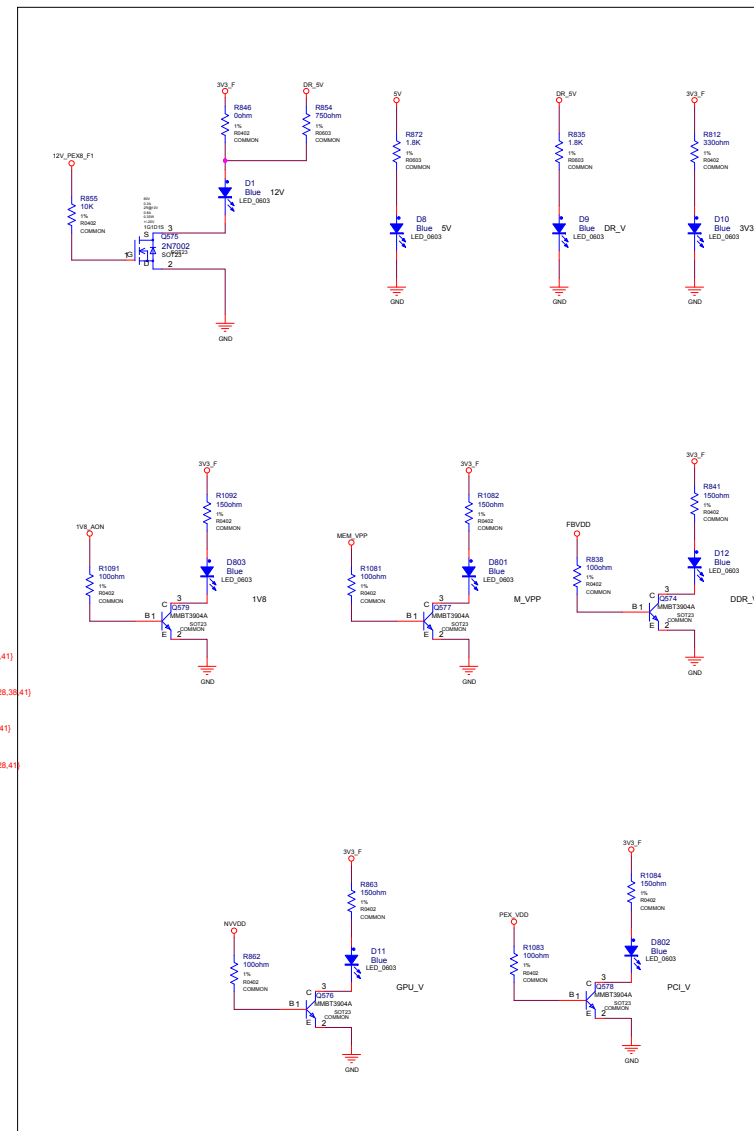
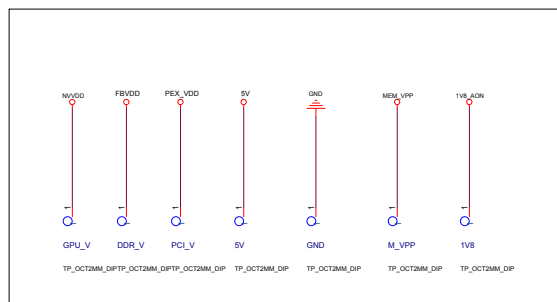
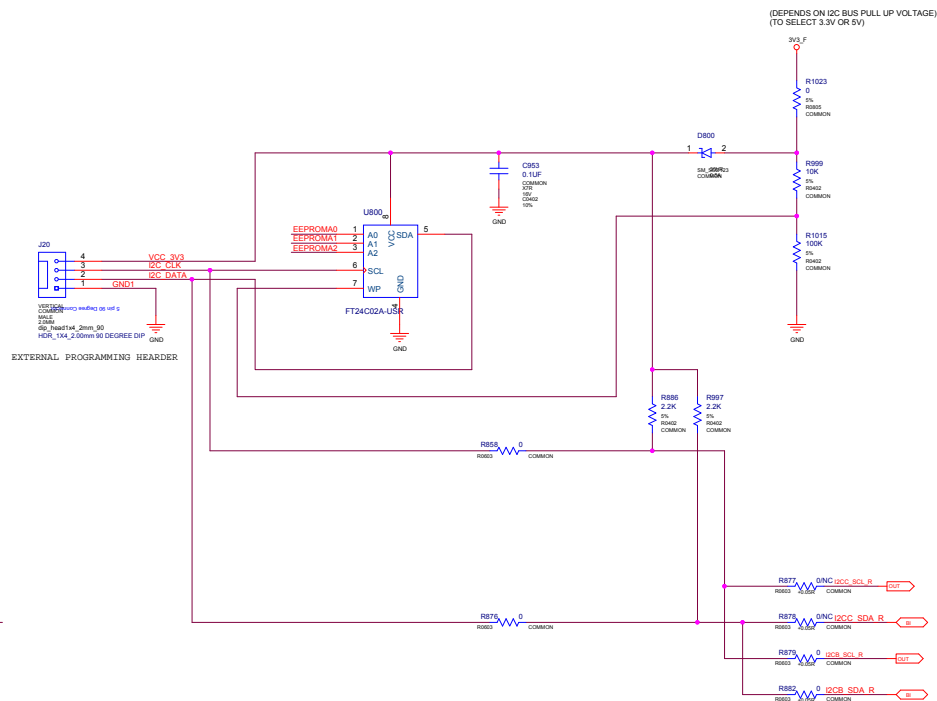
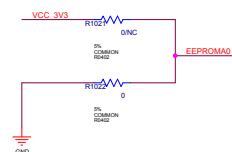
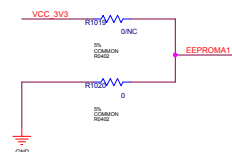
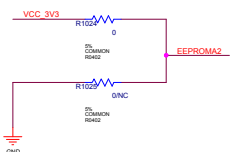


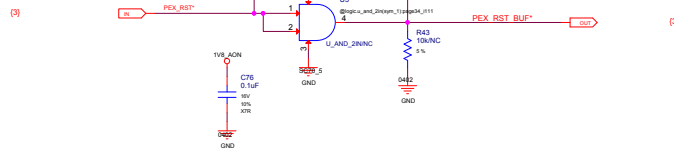
A	B	C	D	E	F	G	PROPERTY NOTE: This document contains information confidential and property to Galaxy Microsystems (HK) Ltd.
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41-PS_VIN-VOUT-LED




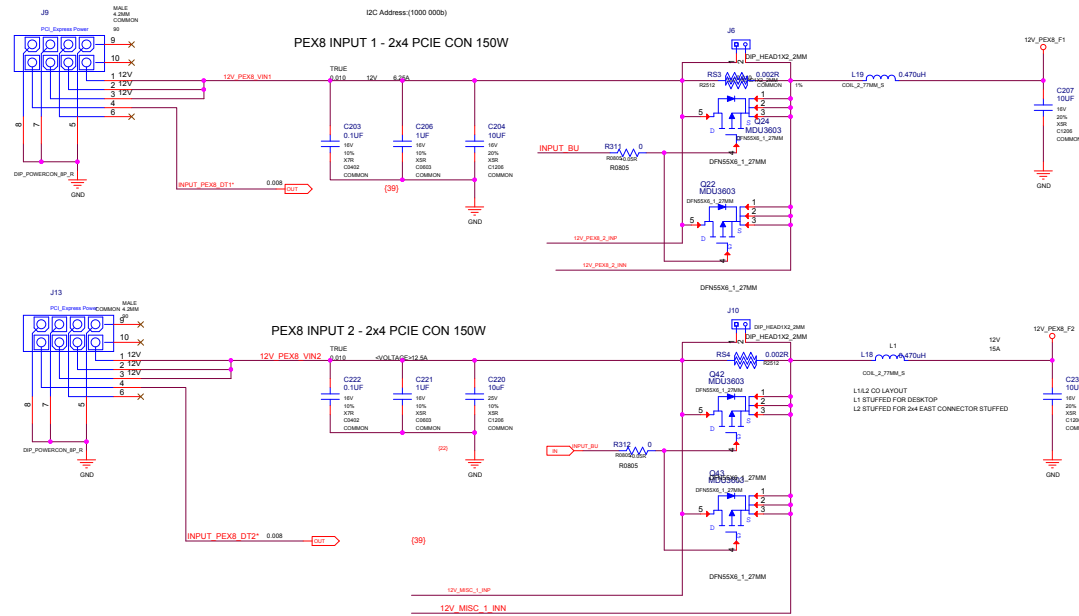
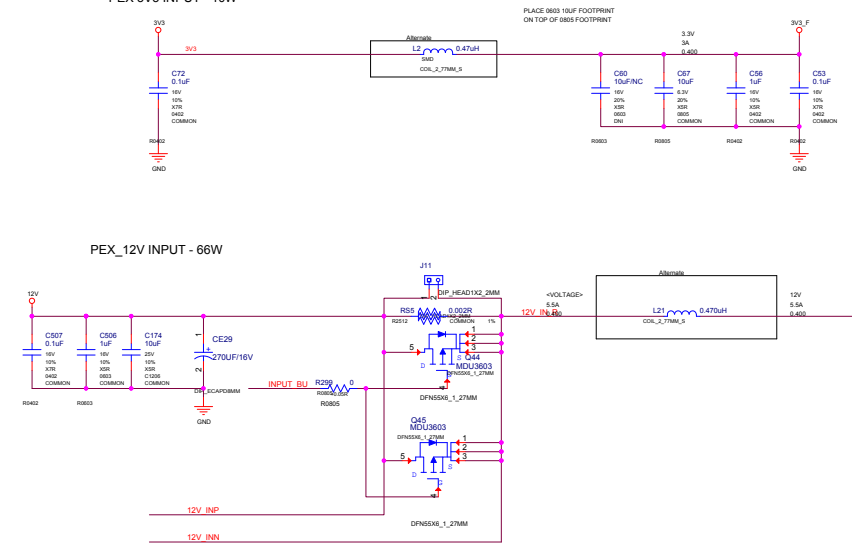
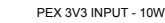
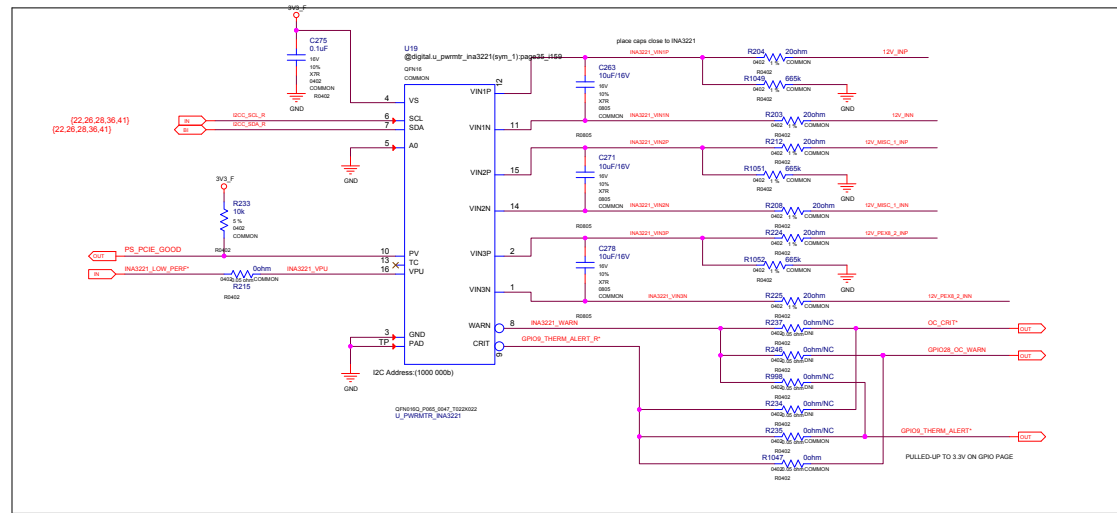
FROM LEFT TO RIGHT : GND,I2C_DATA,I2C_CLK,VCC_3V3






ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NV3V3, NV12V

 GALAXY		Galaxy Microsystems (HK) Ltd.	
Page Name:			
PS: NV3V3, NV12V			
Size Custom	Project Name: P45Z	Design By: Neston	Rev V10
Date: Tuesday, June 21, 2016	Sheet 37 of 41		
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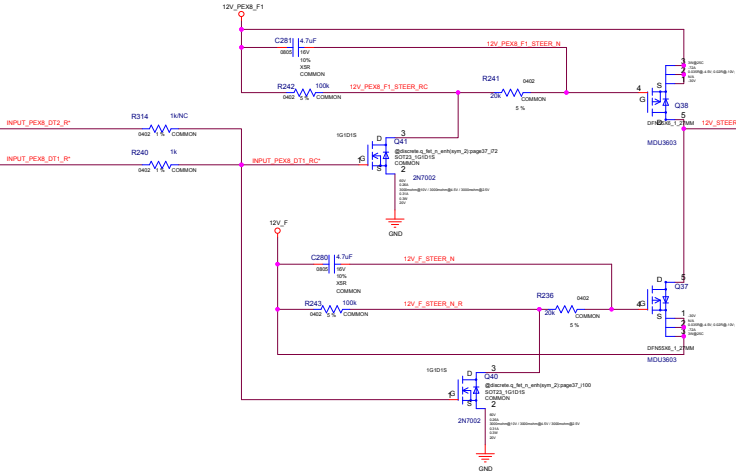




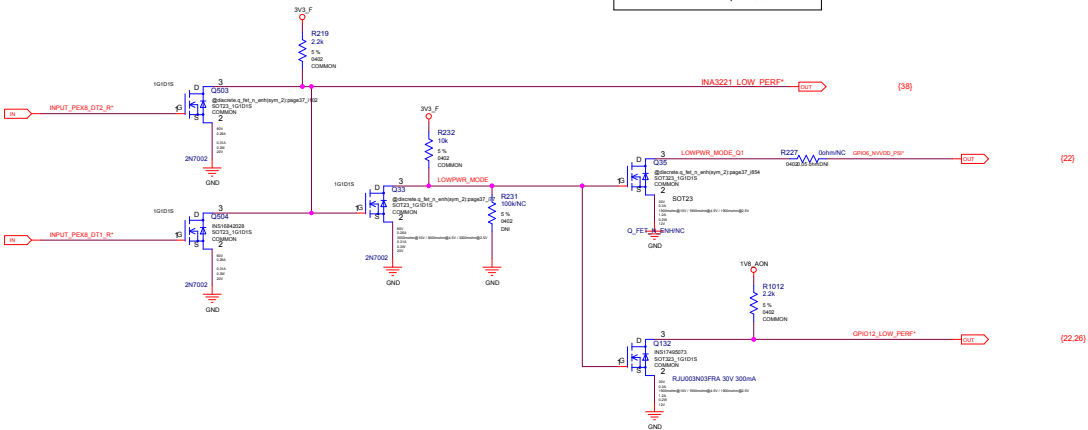
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Shutdown and Sequencing

 GALAXY		Galaxy Microsystems (HK) Ltd.	
Page Name:			
PS: Shutdown and Sequencing			
Size Custom	Project Name: P45Z	Design By: Neston	Rev V10
Date: Tuesday, June 21, 2016		Sheet 39 of 41	
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PEX Input - 12V Current Steering FETs

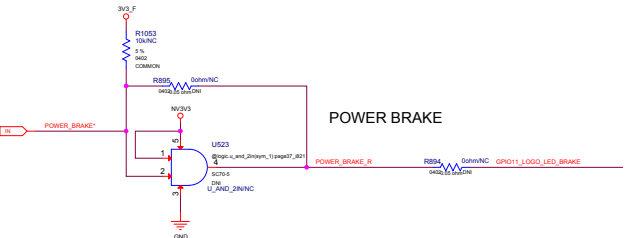


PEX Input - Power Level/PSI* Control

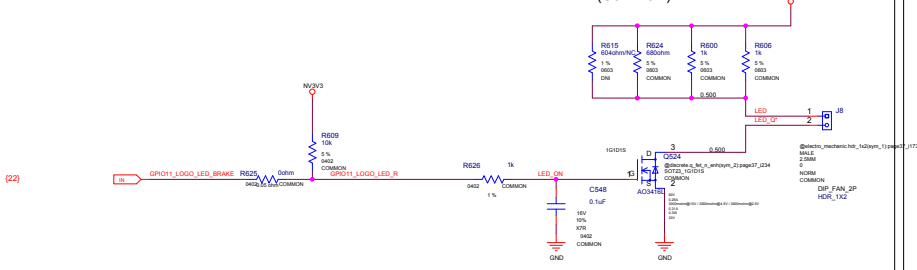


GPI012_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

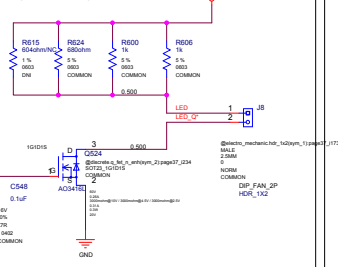
POWER BRAKE



GeForce Logo LED



LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)

